REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Office Action dated April 13, 2006. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 1-23 are under consideration in this application. Claims 1 and 10-11 are being amended, as set forth in the above marked-up presentation of the claim amendments, in order to more particularly define and distinctly claim applicants' invention. New claims 21-23 are being added.

All the amendments to the specification and the claims are supported by the specification, especially the allowed claims. Applicants hereby submit that no new matter is being introduced into the application through the submission of this response.

Allowed Subject Matter

Claims 6-7, 9 and 16 were allowed.

Prior Art Rejections

Claims 1-5, 8, 10-15 and 17-20 were rejected under 35 U.S.C. § 102(a) as being anticipated by US Patent No. 5,907,481 to Svardsjo (hereinafter "Svardsjo"). US Patent No. 6,574,124 to Lin et al. (hereinafter "Lin") was considered pertinent to the application. The above rejection has been carefully considered, but is most respectfully traversed.

The semiconductor integrated circuit of the invention for power supply control performs switching control of a switching power supply device which switches currents flowing through a primary coil of a transformer TS1 for voltage conversion to drive the primary coil with alternate currents and rectifies currents flowing through a secondary coil of the transformer to output DC voltages.

The semiconductor integrated circuit (for example, the 2nd embodiment depicted in Figs. 1-4, 9; pp. 11-24), as now recited in claim 1, generates and outputs a control signal AD3 for dynamically controlling off-timings of a transistor (e.g., M6 or SF, p. 23, last paragraph) for synchronous rectification at the secondary coil in accordance with at least one of an input

voltage Vin of the primary coil and a load current Iout of the secondary coil to turn off the transistor M6 immediately before inverting a current direction flowing through the primary coil Vsec 0. ("*It is most desirable to turn off the switch SF at the timing t5 immediately before the timing t6 that inverts the direction of the current flowing through the coil.*" p. 23, last 4 lines; Fig. 4) so as to minimize switching power losses (p. 3, line 2). In particular, timings of the control signal are variably delayed at delay amounts by a variable delay circuit 33, and said delay amounts are generated by a delay amount control circuit 34 based upon setup information (Fig. 2; claim 6).

The semiconductor integrated circuit (for example, the 2nd embodiment depicted in Fig. 15 & Figs. 16(3)-(4); pp. 34-39), as now recited in claim 10, is configured to selectively set any detection criterion level VBS (Fig. 15) for a circuit to generate a signal (e.g., OUT-B) which detects a voltage between terminals of a switching element (e.g., M2) in a circuit for switching currents flowing through the primary coil and controls on-timings of the switching element M2 at time points when a terminal voltage of the primary coil becomes minimum ("*The MOSFET M2 shifts from the off-state to the on-state at the time point when the coil's terminal voltage V11 becomes minimum (0 V)*" p. 37, lines 16-17; Fig. 16) so as to minimize switching power losses (p. 37, last line). In particular, timings of said switching currents are variably delayed at delay amounts by a variable delay circuit 33, and said delay amounts are generated by a delay amount control circuit 34 based upon setup information.

The invention of claim 11 is directed to a switching power supply device comprising: the semiconductor integrated circuit of claim 1; a transformer for voltage conversion; a switching circuit which switches currents flowing through the primary coil of the transformer for voltage conversion to drive the primary coil with alternate currents; a rectifier circuit including a synchronous rectification transistor and rectifies currents flowing through a secondary coil to output DC voltages, the synchronous rectification transistor being connected between one terminal of the secondary coil of the transformer for voltage conversion and a reference potential terminal and turned on or off in synchronization with switching operations of the switching circuit; a capacitor element for smoothing voltages rectified by the rectifier circuit; a variable delay circuit 33 variably delaying timings of said currents flowing through the primary coil of the transformer by delay amounts; and a delay amount control circuit 34 generating said delay amounts based upon setup information,

An input voltage to the primary coil is divided by resistors and is supplied to the semiconductor integrated circuit for power supply control.

The invention has a full bridge structure in a primary side, and the structure of a second side and PWM control with phase shift is directed to (1) decreasing losses in the rectifier circuit at the secondary side, increasing a switching frequency, and miniaturizing a DC-DC converter ([0011]), and (2) providing a switching power supply device and its control semiconductor integrated circuit capable of optimizing on-timing of a switch element at the primary side and off-timing ([0013]). The invention recited in the claims 1 and 11 reduces power losses at a secondary side for the secondary coil, by the transistor being turned off at the optimal timing in accordance with changes in load currents at the secondary side or the input voltage of the primary coil (p. 5, 2nd paragraph; p. 6, last 2 paragraphs; p. 24, last paragraph). The invention recited in the claim 10 reduces power losses of a primary side for the primary coil by being able to set any detection criterion level (p.5, 3rd paragraph; p. 7, 2nd & 3rd paragraphs). As such, the invention doesn't depend on the input voltage and the output current such that the first side can decrease the switching loss by achieving ZVS (Zero Voltage Switching), and the second side can minimize body diode Mitibicayoson of MOS by the dead time optimization.

Applicants contend that Svardsjo fails to teach or suggest such "a variable delay circuit 33 variably delaying timings of said currents flowing through the primary coil of the transformer by delay amounts; and a delay amount control circuit 34 generating said delay amounts based upon setup information" according to the invention, which were indicated by the Examiner as patentable features on page 3, 1st paragraph of the Office Action dated November 23, 2005.

In contrast, Svardsjo (col. 2, lines 3-7) deliberately avoids such a complex gate drive scheme with the a variable delay circuit 33 and the delay amount control circuit 34 of the invention. Svardsjo's the secondary control supply voltage Vs is obtained at a point a located between the commonly connected second terminals of the first and second rectifying Q3,Q4 (Fig. 2), and Svardsjo's secondary control signal is generated with a simple circuit from the primary control signal (Fig. 4). Since Svardsjo provides synchronous rectification on the second side by an easy circuit composition, and it decreases the loss compared with the diode rectification such that it does not provides control signal timing adjustments (e.g., delay) according to the output current and the input voltage, as does the invention.

As to Lin, Lin's signal of current sense is input to a PWM control circuit 16b and then to a comparator 27b. The current sense is done with a current transformer composed of a transistor instead of a diode (col. 1, line 62 to col. 2, line 39; Figs. 2, 6, 8). Lin's control

signals are not input into any delay control circuit 34 as does the invention (Fig. 1). As such, Lin shares the same deficiencies as Svardsjo.

Applicants contend that the cited references or their combination fail to teach or disclose each and every feature of the present invention as disclosed in the independent claims 1 and 10-11. As such, the present invention as now claimed is distinguishable and thereby allowable over the rejections raised in the Office Action. The withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

Conclusion

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art reference upon which the rejections in the Office Action rely, Applicants respectfully contend that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicants' undersigned representative at the address and phone number indicated below.

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